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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/005,062	12/03/2001	Daniel R. Watkins	LS1-01-651	9196

7590

09/15/2003

LSI Logic Corporation  
Patent Law Department  
M/S D-106  
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EXAMINER

GARBOWSKI, LEIGH M

ART UNIT PAPER NUMBER

2825

DATE MAILED: 09/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/005,062

Applicant(s)

WATKINS, DANIEL R.

Examiner

Leigh Marie Garbowski

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 21-35 is/are allowed.
- 6) ☒ Claim(s) 1,10,11 and 18-20 is/are rejected.
- 7) ☒ Claim(s) 2-9 and 12-17 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)                      4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_.
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)                      5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_.
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Claim Objections***

Claims 3, 11, 13, 23 are objected to because of the following informalities: as per claims 3, 13, 23, "core" [line 2] should be --cores--; as per claim 11, "layer" [line 6] should be --layers--. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,10-11 and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Pedersen et al. [U.S. Patent #6,134,705].

As per claim 1, Pedersen et al. disclose a method for implementing a change to a circuit design for a system formed on a semiconductor chip, the circuit design including at least one circuit core, the method comprising: providing in the circuit design at least one FPGA core [column 7, lines 20-28]; extracting an incremental change to the circuit design by comparing a new RTL design and an old RTL design for the system [column 6, lines 20-26; column 11, lines 7-11]; synthesizing said incremental change into a netlist for said at least one FPGA core [column 9, lines 4-9, 43-45]; generating new metal layer interconnections so as to provide an input and an output for said at least one FPGA core in accordance with said incremental change [column 10, lines 15-17; column 13, lines 53-54]; and programming said at least one FPGA core in accordance

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with the netlist [column 7, lines 31-34]. As per claim 7, Pedersen et al. further disclose wherein said circuit design of a system formed on a chip includes at least one of an ASIC design [column 2, lines 37-38].

As per claim 11, Pedersen et al. disclose a system formed on a semiconductor chip, a circuit design for said system including an incremental change from an old circuit design, said system comprising: at least one circuit core provided on a semiconductor substrate [column 7, lines 20-28]; at least one FPGA core, said at least one FPGA core being programmed and configured to reflect the incremental change [column 7, lines 20-28]; and metal layers formed on the semiconductor substrate, said metal layers having interconnections providing an input and an output for said at least one FPGA core in accordance with the incremental change [column 9, lines 4-9; column 10, lines 15-17]. As per claim 18, Pedersen et al. further disclose wherein said incremental change includes a difference between a new RTL design and an old RTL design for said system [column 6, lines 20-26; column 11, lines 7-11]. As per claim 19, Pedersen further disclose wherein said at least one FPGA core implements a netlist synthesized from said incremental change [column 9, lines 4-9, 43-45]. As per claim 20, Pedersen et al. further disclose wherein said system formed on a chip includes at least one of an ASIC [column 2, lines 37-38].

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Watkins [U.S. Patent #6,434,735 B1] discloses an FPGA core able to be programmed for incremental changes to a design. McElvain et al. [U.S. Patent #6,519,754 B1] disclose allocating an area of an FPGA for implementing an RTL

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netlist. Dillon [U.S. Patent #6,093,214] discloses implementing a design change by inserting backfill cells into a netlist. Parlour [U.S. Patent #5,867,396] discloses comparing old and new netlists in an incremental design process. Morgan [U.S. Patent #6,530,073 B2] discloses generating RTL and gate-level netlists in response to engineering change orders.

***Allowable Subject Matter***

Claims 21-35 are allowed.

The following is an examiner's statement of reasons for allowance: although Pedersen et al. discloses method, as well as an apparatus [column 16, line 66-column 17, line 11] and program storage device [column 17, lines 12-29], as outlined above, Pedersen et al. do not disclose or suggest that the FPGA core is to be placed in an unused area of the chip.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

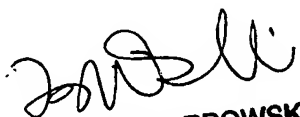
Claims 2-9 and 12-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 703-305-9753. The examiner can normally be reached on days.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 703-308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.

  
LEIGH M. GARBOWSKI  
PRIMARY EXAMINER